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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,335	10/28/2003	Jeffrey P. Gambino	BUR920010040US2	4853

24241 7590 07/25/2005

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/695,335	GAMBINO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on May 13, 2005 has been entered and forwarded to the examiner on May 19, 2005.

Therefore claim 13 as amended by the amendment and claims 14-20 as previously recited are currently pending in the Application.

Claims 1-12 were previously cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Augusto (U.S. Patent No. 5,963,800 herein after Augusto) (previously applied).

With respect to claim 13 , Augusto describes a thin film insulating (Fin) metal oxide semiconductor field effect transistor (MOSFET) comprising: a bottom Si-containing layer, (Augusto col. 10 lines 3-5) an insulating region present atop said bottom Si-containing layer, (Augusto fig. 3 # 5,7 col. 1 1 lines 29-46) said insulating region having at least one partial opening therein, (Augusto figure 3 # 5) a gate region in said partial opening, (Augusto fig. 3 # 13) said gate region comprising two regions of gate conductor that are separated from vertical channel regions by an insulating film, (

Augusto fig. 3 # 13 separated from 3 by 11, vertical channel- title etc.) said insulating film comprising a gate dielectric and having opposite vertical surfaces adjacent to the channel regions, (Augusto e.g. figure 3 gate insulator # 11) source/drain diffusion regions abutting said gate region, (Augusto figure 3 # 5',7' (source) and # 1' (drain) abutting gate 13, col. 2 lines 38-40) said source/drain diffusion regions having junctions that are self-aligned to the vertical channel regions and the gate region', (Augusto e.g. figure 3 # 5',7' (source) and #1',15 (drain) self-aligned with channel 3, 3') and insulating spacers in said partial opening that separate the gate region and the source/drain diffusion N region formed orthogonal to said insulating film. (Augusto figure 3 spacer not numbered orthogonal to gates 13) and wherein said gate region is between said insulating spacers (Augusto figures) and wherein said MOSFET is a double-gated/double-channel MOSFET device. (Augusto e.g figures.) in which the gate region is self-aligned to the source/drain diffusion regions and vertical channel regions. (Augusto e.g. figure 3 # 5',7' (source) and #1',15 (drain) self-aligned with channel 3, 3, col. 2 lines 38-40, col. 12 lines 41-46).

With respect to claim 14 Augusto describes the Fm MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material. (Augusto col. 25 lines 65-66).

With respect to claim 15 Augusto describes the Fm MOSFET of Claim 13 wherein said partial opening exposes a portion of said insulating layer of said SOI material. (Augusto figures 9.4, 15.1,. etc.)

With respect to claim 16 Augusto describes the Fm MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer. (Augusto figure 9.4, 15.1 insulators on sides)

With respect to claim 17 Augusto describes the Fm MOSFET of Claim 16 wherein said gate dielectric is comprised of an oxide, a nitride, an oxy nitride or any combination or multi layer thereof. (Augusto figure 15.1 , col. 27 lines 5-65).

With respect to claim 18 Augusto describes the Fm MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multi layers thereof. (Augusto col. 6 line 50 and PMOS or NMOS by definiation is a metal gate, figure 8.3 etc.)

With respect to claim 19 Augusto describes the Fm MOSFET of Claim 13 further comprising silicide regions formed atop said source/drain àiffusion regions. (Augusto col. 6 line 50). With respect to claim 20 Augusto describes the Fm MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer. (Augusto figure 7 (s) and (d) formed in patterned Si containing layer).

Response to Arguments

Applicant's arguments filed 02/02/05 have been fully considered but they are not persuasive for the following reasons.

Applicants' first contention that Augusto does not teach or suggest vertical channels is not persuasive because Augusto in its title , abstract and description , etc.

repeatidly refers to its devices as vertical devices and its title is " CMOS integration process having Vertical Channel. Therefore it is not understood how Applicants' can state Augusto does not teach or suggest vertical channels.

Applicants' second contention that Augusto does not teach suggest a double-gated/ double channel MOSFET device is not persuasive because as show in above Augusto at least in figures and col. 12 lines 54, lines 1-10, etc. describes /suggests a double-gated/ double channel MOSFET device.

Applicants' third contention that Augusto does not teach/ suggest a double-gated/ double channel MOSFET device (see above under second contention) in which the gate region is self-aligned to the source/drain diffusion regions and channel regions is not persuasive (Augusto e.g. figure 3 # 5',7' (source) and #1',15 (drain) self-aligned with channel 3, 3, col. 2 lines 38-40, col. 12 lines 41-46).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao
Patent Examiner
July 20, 2005.

LONG PHAM
PRIMARY EXAMINER